What is claimed is:

1. A method for operating a synchronous memory comprising:
performing an initialization operation on the synchronous memory;
setting a content of a status register to a first state while the initialization operation is being performed; and
setting the content of the status register to a second state when the initialization operation is completed.

2. The method of claim 1 wherein the initialization operation is performed in response to an externally provided signal.

3. The method of claim 1 further comprises outputting the contents of the status register on an external connection in response to a status register read command.

4. The method of claim 1 wherein the initialization operation comprises:
reading data stored in non-volatile fuse elements; and
storing the data read from the non-volatile elements in at least one data register.

5. The method of claim 1 wherein the first state is a logical 1 and the second state is a logical 0.

6. A method for operating a memory system comprising:
initiating an initialization operation on a synchronous memory;
setting a first bit of a status register of the synchronous memory to a first state when the initialization operation is initiated;
setting the first bit of the status register to a second state when the initialization operation is completed;
providing a status register read command with an external memory controller; and

outputting the contents of the status register on an external connection in response to the status register read command.

7. The method of claim 6 wherein the initialization operation comprises:
reading data stored in non-volatile fuse elements; and
storing the data read from the non-volatile elements in at least one data register.

8. The method of claim 6 wherein the initialization operation is performed in response to an externally provided signal from the memory controller.

9. The method of claim 6 wherein the synchronous memory is a non-volatile memory.

10. The method of claim 9 wherein the non-volatile memory is a flash memory.

11. A method for operating a memory system comprising:
initiating an initialization operation on a memory device; and
monitoring a memory status register to determine when the initialization operation is completed.

12. The method of claim 11 wherein initiating and monitoring is performed by a memory controller coupled to the memory device.

13. The method of claim 11 wherein monitoring the memory status register comprises:
performing a status read command on the status register;
determining a state of a first bit of the status register; and
if the first bit is in a predetermined state, indicating that the initialization operation has ended.

14. The method of claim 11 wherein monitoring the memory status register comprises:

performing a status read command on the status register;

determining a state of a plurality of bits of the status register; and

if each of the plurality of bits are in predetermined states, indicating that the initialization operation has ended.

15. The method of claim 11 and further including outputting the memory status register to a data output connection.

16. The method of claim 11 wherein the memory device is compatible with synchronous dynamic random access memory package pin assignments.

17. The method of claim 14 wherein a memory controller performs the status read command and determines the state of the plurality of bits.

18. The method of claim 13 wherein monitoring the memory status register is performed by a memory controller over a bidirectional data bus.

19. The method of claim 11 wherein the initialization operation on the memory device is performed by an internal state machine.

20. The method of claim 11 wherein the memory status register is updated in response to completion of the initialization operation and synchronous with a clock signal coupled to the memory device.